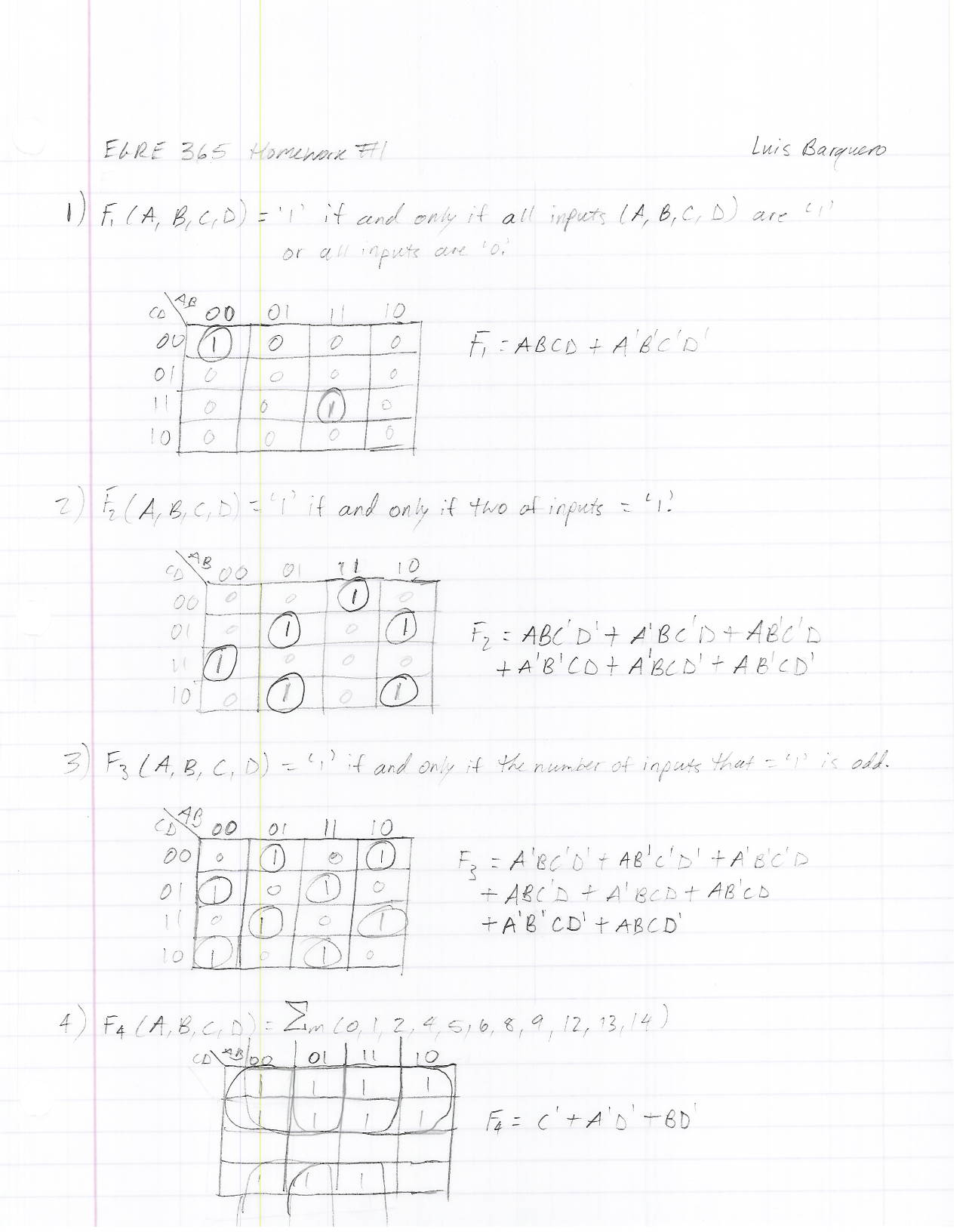
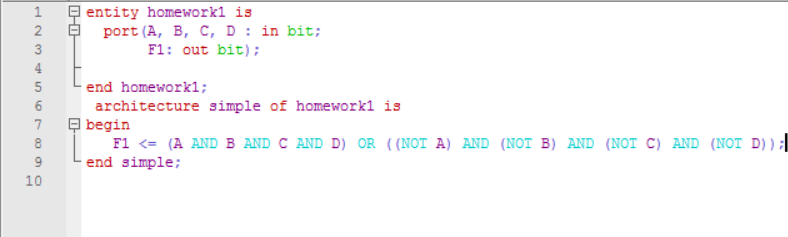
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Homework #1

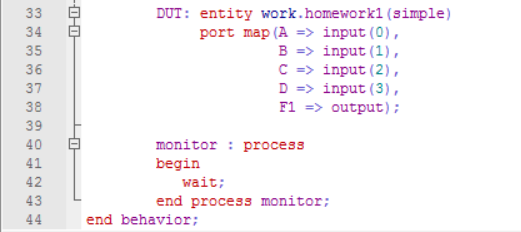
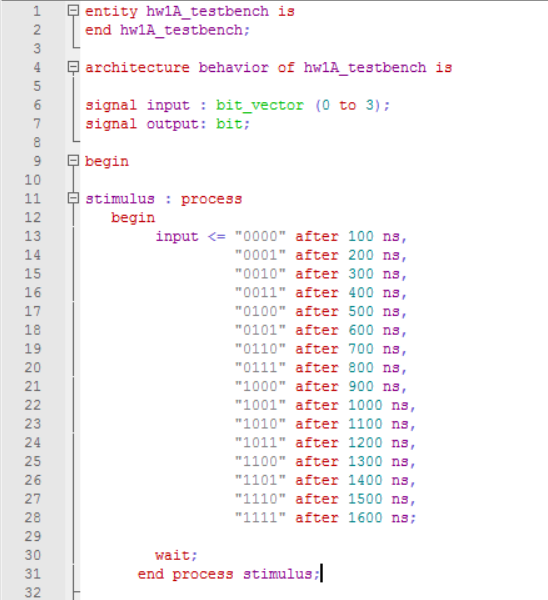
Due: 09/18/17



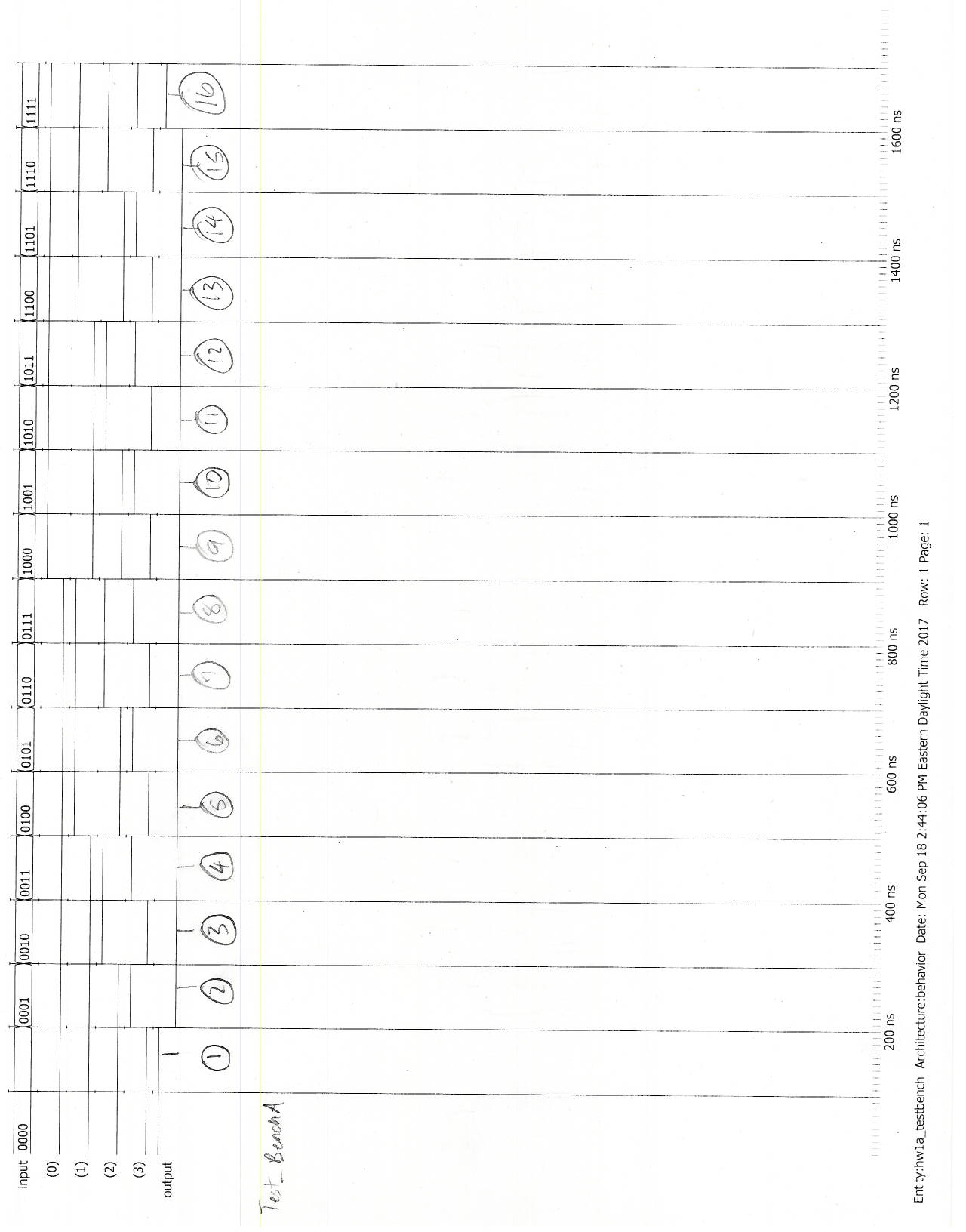
***Figure 1 – Figure one contains question 1’s K-Maps and their corresponding output function.***



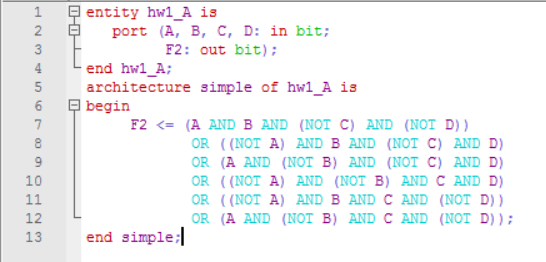
***Figure 2 – Figure 2 contains the code for the F1’s VHDL Model.***



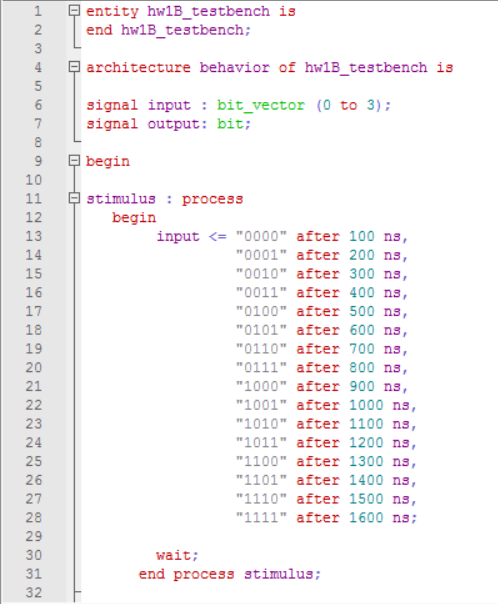
***Figure 3 – Figure 3 contains the code for F1’s Testbench.***

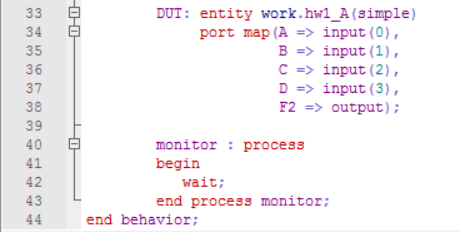


***Figure 4 – Figure 4 contains the simulation result from F1’s testbench.***

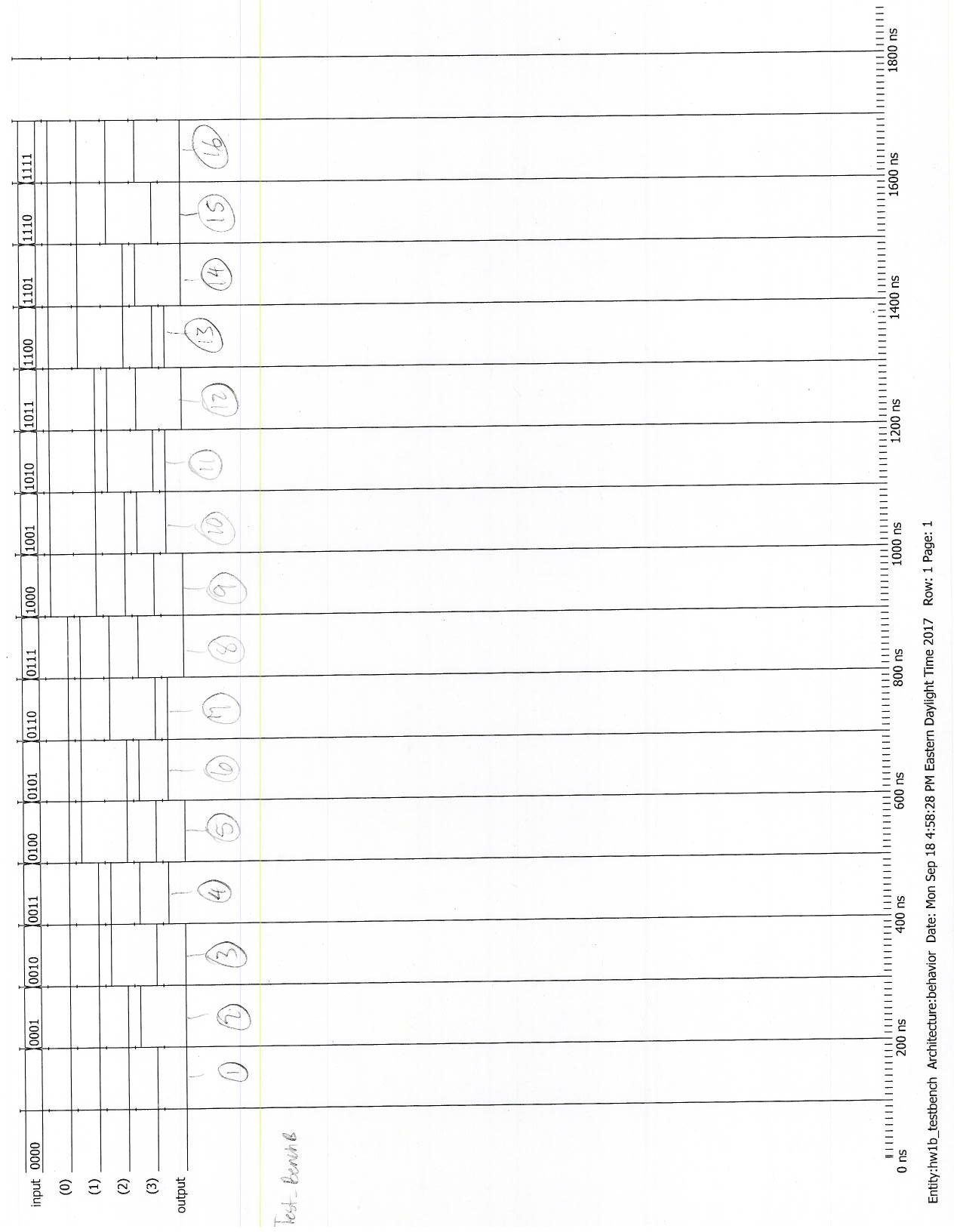


***Figure 5 – Figure 5 contains the code for F2’s VHDL Model***

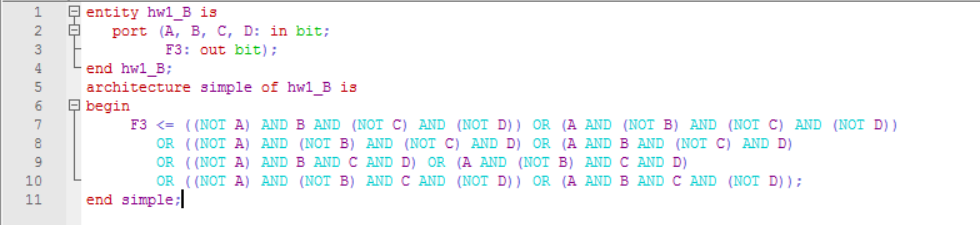




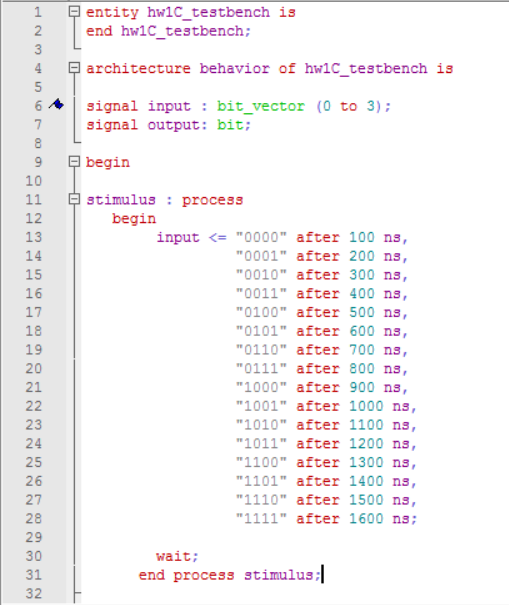
***Figure 6 – Figure 6 contains F2’s VHDL Testbench code.***

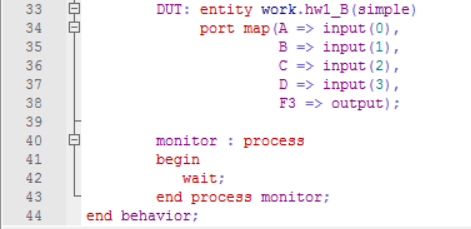


***Figure 7 – Figure 7 contains the simulation result for F2’s VHDL Testbench.***

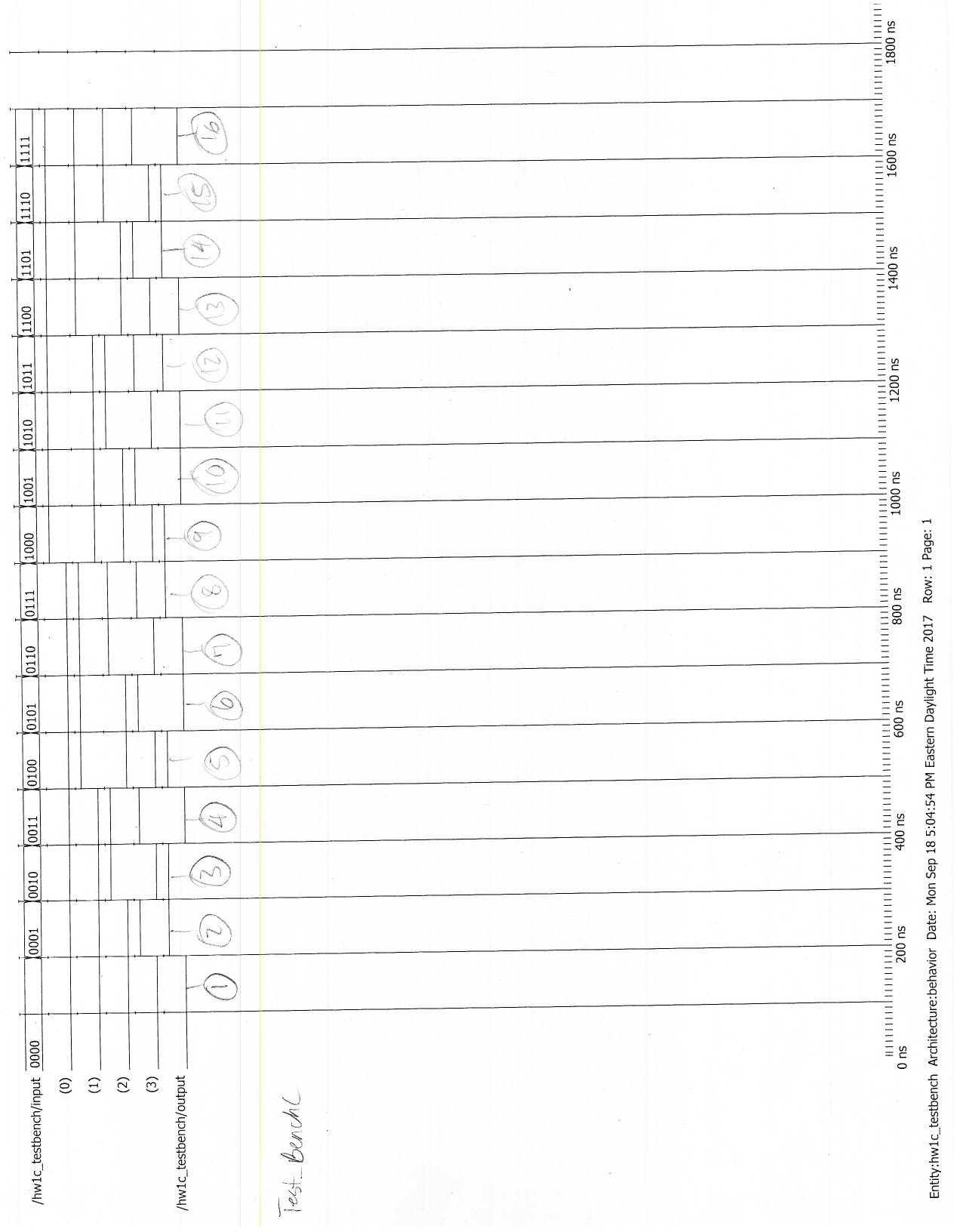


***Figure 8 – Figure 8 contains F3’s VHDL Model code.***

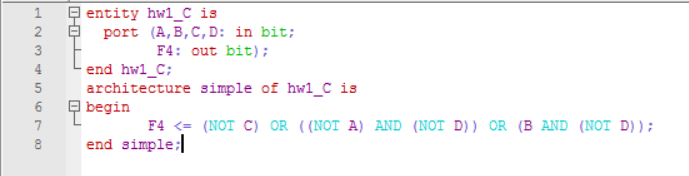




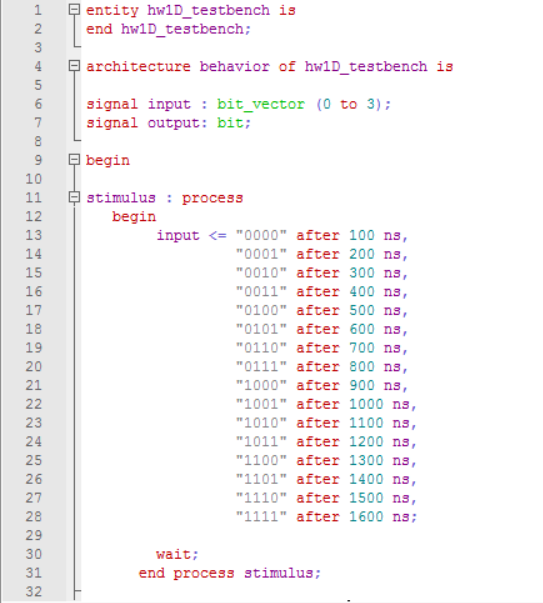
***Figure 9 – Figure 9 contains the F3’s VHDL Testbench Model code.***

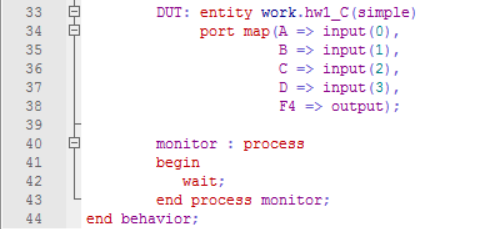


***Figure 10 – Figure 10 contains the simulation result for F3’s VHDL Testbench.***

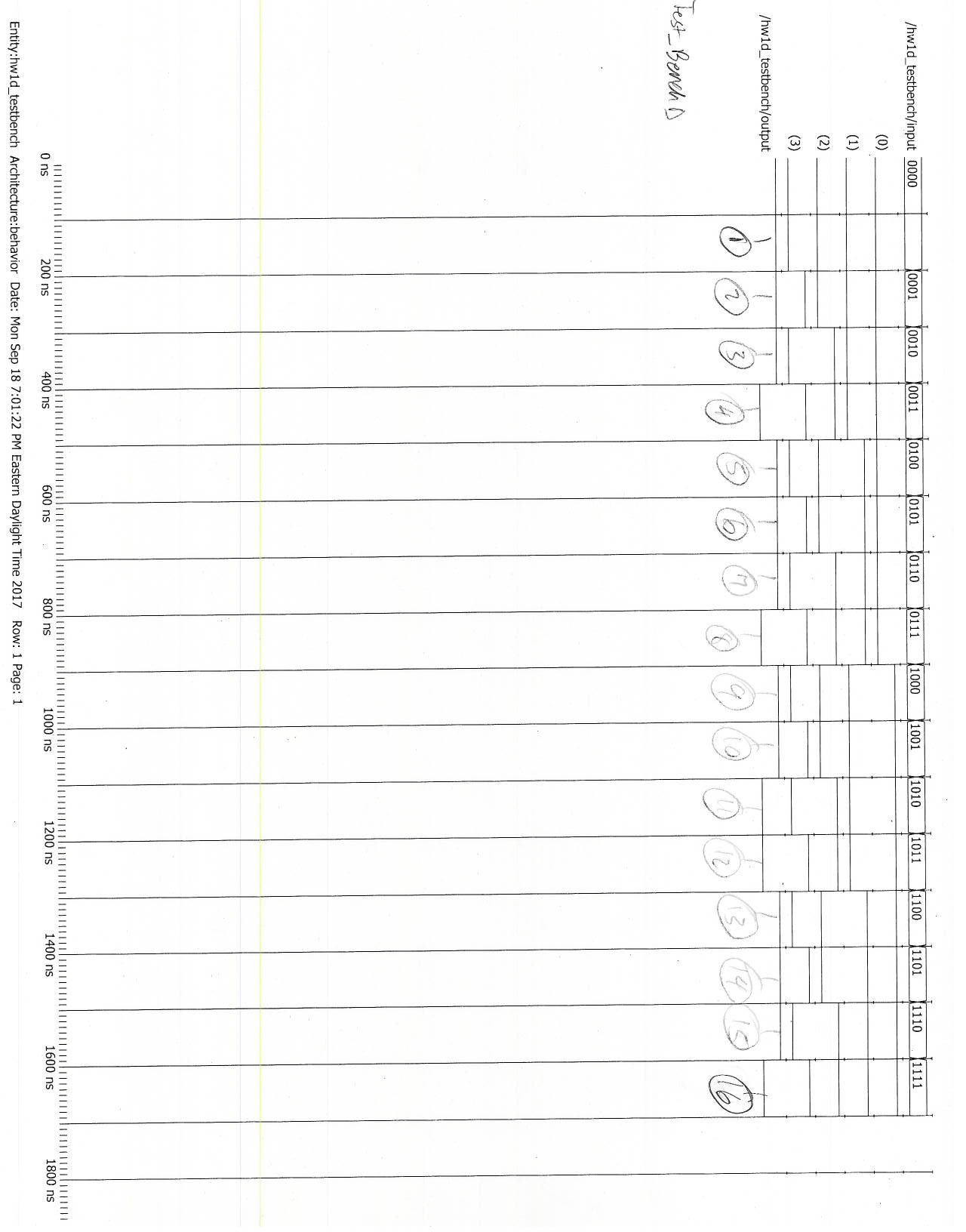


***Figure 11 – Figure 11 contains the code for F4’s VHDL model.***

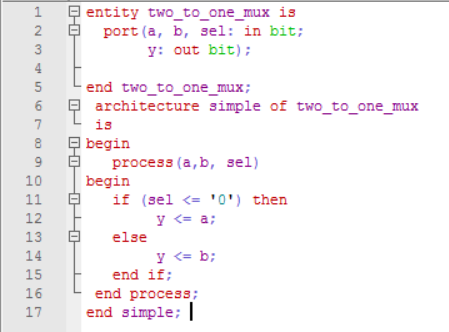




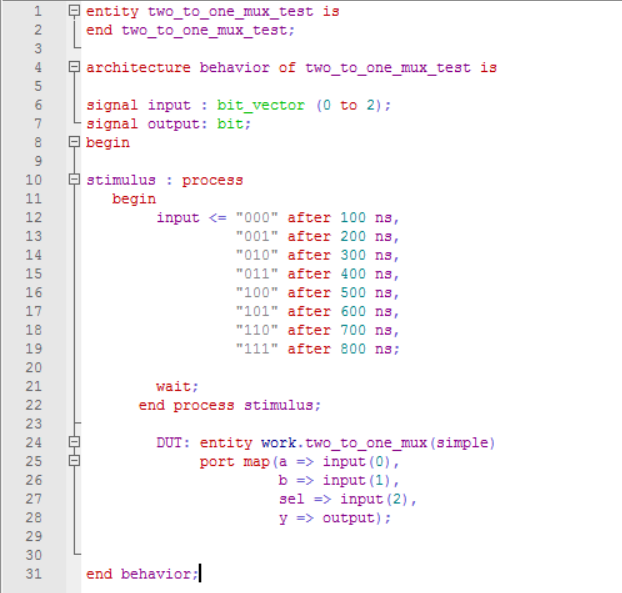
***Figure 12 – Figure 12 contains F4’s VHDL Testbench Model code.***



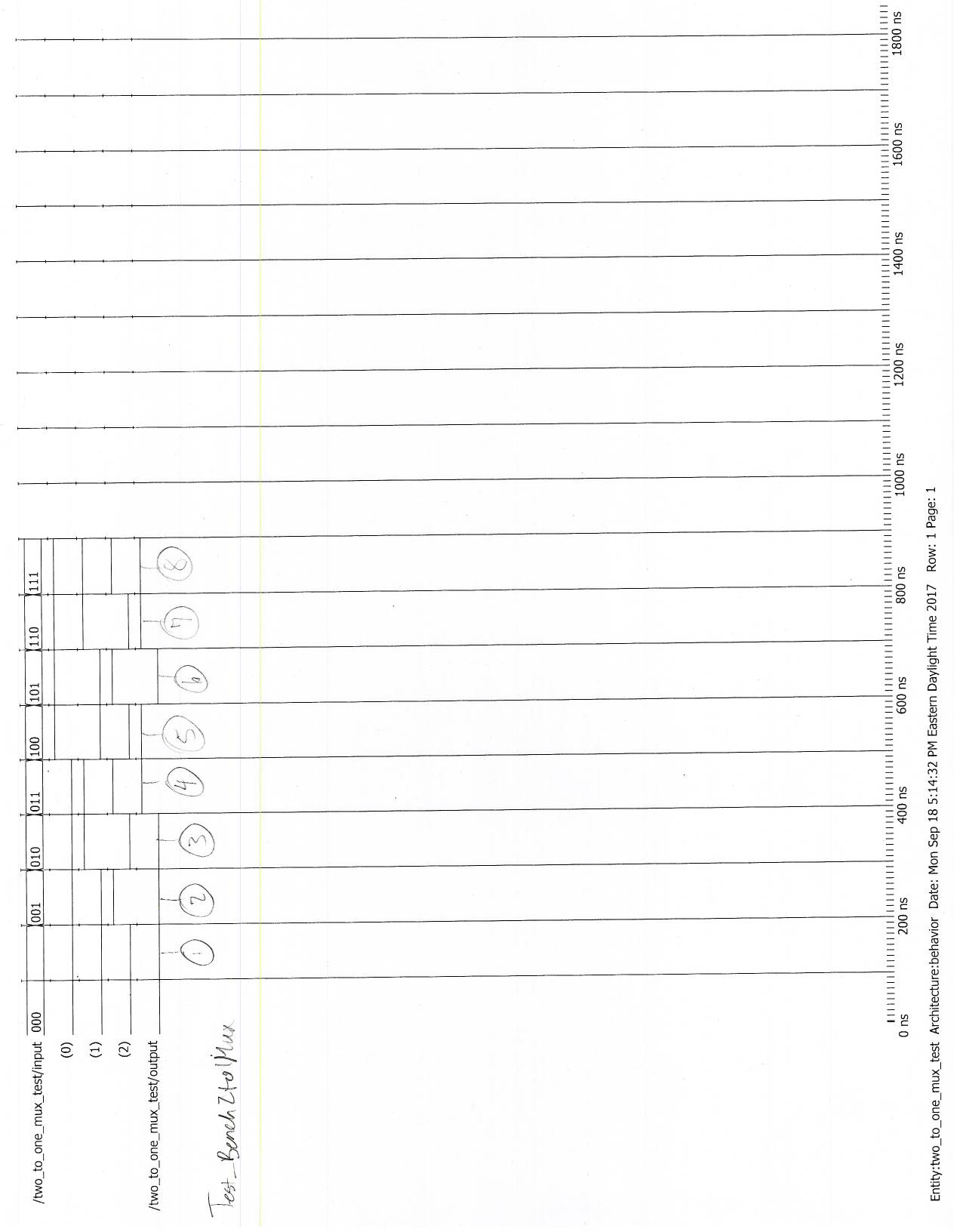
***Figure 13 – Figure 13 contains the simulation result for F4’s VHDL Testbench.***



***Figure 14 – Figure 14 contains the 2-to-1 Mux’s VHDL Model code.***



***Figure 15 – Figure 15 contains the 2-to-1 Mux’s VHDL Testbench Model code.***



***Figure 16 – Figure 16 shows the simulation result for the 2-to-1 Mux’s Testbench.***